Processor reset state

Upon power-up and/or assertion of the RESET# line, the processor is to enter a reset state in which all registers besides IP, SP, FP, TP, GP and ZP (which are initialized to zero) are to be initialized to a value of 0x1A1A1A1A1A1A1A1A. The instruction pointer (IP) being at zero maps to the platform firmware ROM (PFR).

There are two kinds of resets, a **cold** reset and a **warm** reset. A **cold** reset is when power is first applied to the System-on-Chip (SoC) package and results in the processor entering a low-power state in which IP is inhibited until an implementation specific signal tells it to run. A **warm** reset is when power is already applied to the SoC package and the processor reset line is pulled low, in which case doesn't require IP to be inhibited, thus the processor simply runs.

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