Processor registers

YiffCore utilizes 32 general-purpose registers for various data movement operations, to differentiate between temporaries and other registers, the temporaries are known as CUM stores (the SoC has many holes :3):

ZR	:	Fixed to zero, writes are ignored	: ID=0x00
CUM0	:	Temporary data	: ID=0x01
CUM1	:	Temporary data	: ID=0x02
CUM2	:	Temporary data	: ID=0x03
CUM3	:	Temporary data	: ID=0x04
CUM4	:	Temporary data	: ID=0x05
CUM5	:	Temporary data	: ID=0x06
SP	:	Stack pointer	: ID=0x07
FP	:	Frame pointer	: ID=0x08
TP	:	Per-thread data pointer	: ID=0x09
GP	:	Global data pointer	: ID=0x0A
RA	:	Return address	: ID=0x0B
A0	:	Function argument 1	: ID=0x0C
A1	:	Function argument 2	: ID=0x0D
A2	:	Function argument 3	: ID=0x0E
A3	:	Function argument 4	: ID=0x0F
A4	:	Function argument 5	: ID=0x10
A5	:	Function argument 6	: ID=0x11
S0	:	Saved register 0	: ID=0x12
S1	:	Saved register 1	: ID=0x13
S2	:	Saved register 2	: ID=0x14
S3	:	Saved register 3	: ID=0x15
S4	:	Saved register 4	: ID=0x16
S5	:	Saved register 5	: ID=0x17
S6	:	Saved register 6	: ID=0x18
S7	:	Saved register 7	: ID=0x19
S8	:	Saved register 8	: ID=0x1A
S9	:	Saved register 9	: ID=0x1B
S10	:	Saved register 10	: ID=0x1C
S11	:	Saved register 11	: ID=0x1D
S12	:	Saved register 12	: ID=0x1E
S13	:	Saved register 13	: ID=0x1F

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