

Introduction

YiffCore is a 64-bit System-on-Chip architecture targeting low-power embedded systems within the scope of Yiffware infrastructure. YiffCore utilizes 32-bit fixed-width instructions and a handful of registers used to perform data operations. The bus in-use is to have a word-size of 64-bits and be linearly addressed.

Cores are simply needy kitties who sniff around the address space for opcodes to crunch, therefore, individual processing units are referred to as "kits".

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